FULL PAPER

Room-Temperature Printing of Organic Thin-Film Transistors with π-Junction Gold Nanoparticles

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Printing semiconductor devices under ambient atmospheric conditions is a promising method for the large-area, low-cost fabrication of flexible electronic products. However, processes conducted at temperatures greater than 150 °C are typically used for printed electronics, which prevents the use of common flexible substrates because of the distortion caused by heat. The present report describes a method for the room-temperature printing of electronics, which allows thin-film electronic devices to be printed at room temperature without the application of heat. The development of π-junction gold nanoparticles as the electrode material permits the room-temperature deposition of a conductive metal layer. Room-temperature patterning methods are also developed for the Au ink electrodes and an active organic semiconductor layer, which enables the fabrication of organic thin-film transistors through room-temperature printing. The transistor devices printed at room temperature exhibit average field-effect mobilities of 7.9 and 2.5 $cm^2 V^{-1} s^{-1}$ on plastic and paper substrates, respectively. These results suggest that this fabrication method is very promising as a core technology for low-cost and high-performance printed electronics.

1. Introduction

Recent advancements in smart phone and tablet technology have improved mobile devices, and interactive operation through touch-panel displays is a common operating method for electronic products. These developments increase the importance of the role of the display screen, which is becoming wider and thinner with greater resolution and lower electricity consumption. Low field-effect mobility of amorphous silicon thin-film transistors (a-Si TFTs) is a current limitation for the development of high-end displays. Low-temperature polysilicon (LTPS) and oxide semiconductors, such as InGaZnO (IGZO), have been developed because of their relatively greater mobility.[1–3] However, their compricated fabrication process and low yield ratio increase the production cost. Thus, high-mobility TFT devices fabricated using a facile and low-cost method is now desired.

Printed electronics is an emergent subject for the low-cost and large-area fabrication of flexible electronic devices.[4–16] Direct printing of organic thin-film transistors (OTFTs) using soluble organic semiconductors is a particularly promising fabrication method that offers lower production costs, reduced energy consumption, and a smaller environmental burden. Fully-printed OTFTs have been realized by several groups, but the proposed processes still involve some fundamental problems such as poor field-effect mobility (μ_{FET}) and low reproducibility.[6,13–16] We consider that the low reproducibility mainly belongs to the process of electrode formation, where Ag nanoparticle (NP) ink is commonly used as the electrode material. This process is actually not compatible to a common flexible substrate because the high processing temperature of ~150 °C causes significant distortion to the substrate. For instance, a heat shrinkage rate of a plastic film such as polyethylene terephthalate (PET) or polyethylene naphthalate (PEN) is ~2% at 150 °C, resulting in 20 millimeter shrink for a 1-meter-long substrate after annealing at 150 °C. The thermal deformation prevents high-resolution patterning and accurate alignment among the different layers of devices on a flexible substrate. This problem becomes more significant as the production size increases.

This report describes the room-temperature (RT) preparation of fully-printed OTFTs involving the formation and patterning of all layers of the devices. To achieve this RT process, novel Au NPs, which exhibit low resistivity of ~9×10^{-6} Ω cm even after RT deposition and drying without use of an annealing process, were developed. High-resolution patterning methods also were developed for the Au NP ink and an organic semiconductor using the surface wettability difference. Thus, high-resolution patterning of OTFT devices on a non-heat-resistant substrate was achieved by RT printing. The Au NP electrodes also improved charge injection into the semiconductor layer,

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resulting in an average μ_{FET} of 7.9 cm^2 V^{-1} s^{-1} in the OTFT devices formed on a plastic substrate. This value is ten times higher than that of conventional a-Si TFTs and even comparable to that of IGZO TFTs, which warrants use of the printed OTFTs in practical high-end display devices. The RT process also enables printing of OTFT devices on paper, with an average μ_{FET} of 2.5 cm^2 V^{-1} s^{-1}. The proposed technique has potential applications to other thin-film devices, such as organic photovoltaic cells, and may become a fundamental technology in future printed electronics.

2. π-Junction Au Nanoparticles

The critical difficulty in achieving a process for RT printed electronics is the high-temperature annealing process required for metal electrode deposition using metal NP ink. A conventional metal NP ink contains a non-conductive material as the ligand. High-temperature annealing is required to remove it and sinter the metal cores to obtain a conductive metal film. Therefore, we developed π-junction Au NPs for the RT printing of the metal electrodes.[17,18] The concept for this process and the principle behind the Au NP ink are shown in **Figure 1**. The Au NPs possess a metal core surrounded by aromatic molecules as the conductive ligand (Figure 1a), which is the biggest difference between the new inks and conventional metal NP inks. We employed a derivative of metal-free phthalocyanine as the conductive ligand, which has the highly planer molecular structure and large π-conjugated system. The planer structure enables a close contact between the NPs without acting as the steric barrier. The large π-conjugated system is also essential for improving the electrical pathway among the NPs. In the π-junction NPs, orbital hybridization between the π orbitals of the aromatic ligand and orbitals of the metal core contributes charge transport among the NPs. Thus, conductive film can be obtained by RT deposition of the ink without removal of the ligand by annealing. A scanning electron microscopic image of the Au NPs deposited on a substrate is shown in Figure 1b. The Au NPs clearly have a spherical shape that is maintained in the film. However, it exhibits low resistivity of ~9×10^{-6} Ω cm, which is of the same order of magnitude as that of pure Au of 2.2×10^{-6} Ω cm, without the sintering process because of the smooth charge transport among NPs through the conductive ligands. Thus, the Au NP film can be used as the electrode material for the RT printing method. For fabrication of the printed OTFTs using the Au NP ink, a stack of four layers, including source/drain, organic semiconductor, gate dielectric, and gate electrode layers, was prepared to complete the devices, and the RT process was employed for all layers (Figure 1c). Therefore, the OTFTs were fabricated at RT by solution-based methods without any heat application during the fabrication processes.

3. Fabrication of OTFT Arrays

A surface selective deposition method was used to pattern the Au NP ink on the substrate.[14,19] For this method, selective regions on the hydrophobic polymer surface were exposed to vacuum ultraviolet (VUV) light to transform the surface into a hydrophilic, wettable surface. The VUV exposure under air generates oxygen radicals and ozone molecules, which cause chemical bond dissociation at the polymer surface and render the region hydrophilic, resulting in patterned wettability. The VUV irradiation system was composed of a Xe excimer lamp as the VUV light source (wavelength of 172 nm, Figure S1a-b) and a mask aligner, which allows selected regions on the surface to be exposed to the VUV light through a photo mask under ambient atmospheric conditions. The Au NP ink was deposited by spreading the ink onto the patterned surface using an applicator to obtain the patterned metal layer (Figure S1c). The

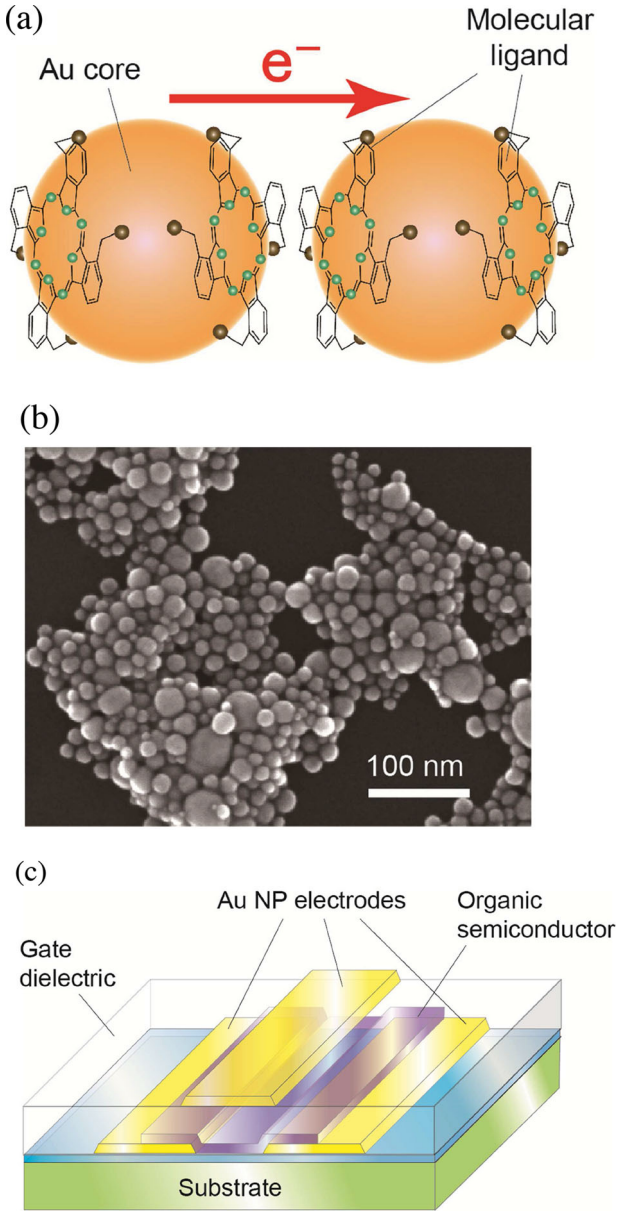

Figure 1. a) Schematic illustration of π-junction Au NPs. The metal core is surrounded by aromatic molecular ligands. b) Scanning electron microscope image of Au NPs deposited on a substrate. c) Structure of OTFT devices fabricated by the RT printing process.

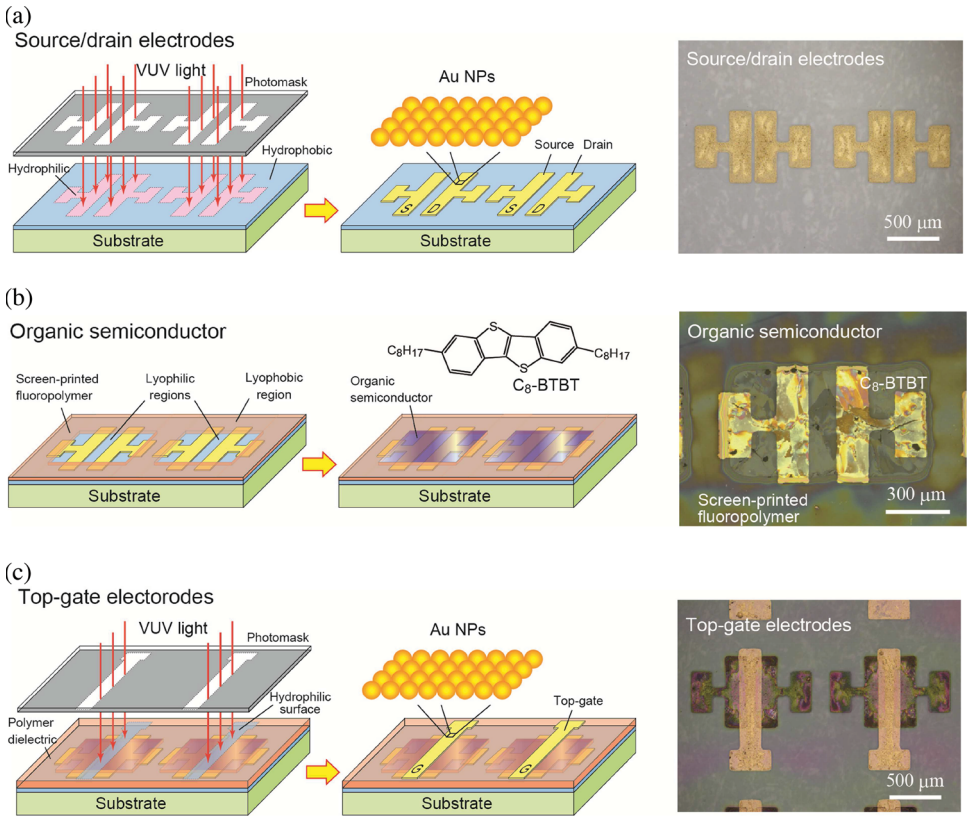

Figure 2. Schematic illustration of OTFT array fabrication using the RT printing method. a) Formation of source/drain electrodes on a hydrophobic surface using: (i) Selective wettability patterning by VUV irradiation of the source/drain electrode regions to render them hydrophilic (left); and (ii) selective deposition of Au NP ink on the hydrophilic regions to form the source/drain electrodes (center). Picture on the right is an optical micrograph of the source/drain electrodes formed by the selective deposition method. b) Formation of organic semiconductor layers using screen printing and solution casting: (iii) The fluorinated polymer layer was screen-printed out of the channel region as a guide for the organic semiconductor deposition (left). (iv) Drop casting of a C_8-BTBT solution onto the surface to selectively crystallize the molecules only in the channel region (center). Picture on the right is an optical image of the organic semiconductor film patterned by this method. c) Patterning of the top-gate electrodes by (v) VUV irradiation of the gate electrode regions on the gate insulator to render them hydrophilic (left). (vi) Formation of top-gate electrodes by application of Au NP ink to the hydrophilic regions (center). Picture on the right is an optical image of the TFT devices after formation of the top-gate electrodes.

highest resolution achieved by this method was 10 μm for a line or space (Figure S1d-e).

Figure 2 illustrates the RT printing process of OTFT arrays. We used a PEN film with a surface planarizing layer of parylene as the flexible plastic substrate. The source/drain electrodes, an organic semiconductor layer, and gate electrodes were fully patterned using a solution-based printing method at RT. First, the source/drain electrode patterning was performed on the hydrophobic substrate surface. The source/drain regions on the surface were exposed to VUV irradiation through a photo mask under ambient atmospheric conditions to render the exposed surface area hydrophilic. After surface wettability patterning, the Au NP ink was applied to the surface, resulting in a pattern of Au ink only on the hydrophilic regions. The Au ink dried in several seconds at RT, and the source/drain electrode layer was obtained using a RT process (Figure 2a).

Then the organic semiconductor layer was added onto the channel region of the devices using a two-step printing processes, screen printing and solution casting (Figure 2b). On the source/drain electrode layer, first a fluorinated polymer layer of Cytop (Asahi Grass Co. Ltd.) was formed around the channel region of OTFTs by screen printing. Then, the Cytop was dried at RT without annealing, resulting in a uniform polymer layer 120 nm thick. The lyophobic nature of the fluorinated polymer surface inhibits deposition of organic semiconductor. Therefore, it acts as a guide for the organic semiconductor solution. Semiconductor layer deposition was performed next, through simple drop casting of 0.5 wt% chlorobenzene solution of dioctylbenzothienobenzothiophene (C_8-BTBT)[20,21] into the lyophilic channel region. Because of the highly repellent nature of the Cytop surface, the semiconductor solution was deposited only on the channel regions, and a patterned organic layer was formed after solvent evaporation. The high boiling point solvent allows formation of a uniform semiconductor layer with relatively large grain size of ~100 μm.

The bilayer structure was used for the gate dielectric. Here, Cytop is used as the interfacial layer at the organic semiconductor/gate dielectric interface.[22,23] Charges accumulate in the vicinity of the interface in OTFTs, and a hydrophobic polymer or self-assembled monolayer is useful for modifying the interface and reducing charge trapping in the channel region.[22–24] Introduction of the Cytop layer greatly reduces the trap density at the interface, and suppresses electrical hysteresis behavior of the devices. The role of the second layer is suppression of VUV

penetration into the organic layer during top-gate electrode formation, which degrades device characteristics due to disruption of the organic layer by VUV, in the next step. The upper layer also offers better patterning of the top-gate electrode layer compared to that on the Cytop layer. Two choices exist for the upper gate dielectric: chemical vapor deposition of parylene or spin coating of the fluorinated polymer Fluorosurf (Fluoro Tech Co. Ltd.). The parylene layer provides better patterning of top-gate electrodes in the next step, but a chemical vapor deposition process under vacuum is necessary to form it. The fluorinated polymer can be formed by spin coating and dries naturally at room temperature without applying heat, but requires a longer VUV irradiation time and results in lower resolution of the patterning of the top-gate layer, probably due to greater surface roughness and lower VUV absorbance. In contrast, both of the gate dielectrics result in similar OTFT performance.

The last step was patterning of the top-gate electrode layer, accomplished by VUV exposure. The gate electrode regions on the gate dielectric were exposed to VUV light through a photo mask to render them hydrophilic, followed by application of Au NP ink using the applicator to selectively deposit it only onto the hydrophilic regions. The Au NPs were dried at RT without application of heat (Figure 2c).

Results of RT printing of OTFT arrays on the flexible plastic substrate are shown in **Figure 3**. Since a flexible material was used for all of the layers, the array obtained was a fully flexible OTFT array, as shown in Figure 3a. The optical micrograph of the fully-printed OTFT array obtained by RT printing is also shown in Figure 3a. The electrode and semiconductor layers were completely patterned for complete isolation among the devices, which is essential for reducing gate leakage current and inter-device crosstalk (Figure 3b).

4. Electrical Performance of the Room-Temperature Printed OTFTs

The results of electrical characterization for RT-printed OTFTs are shown in Figure 3c and d. The nonlinear increase in drain current in the low-drain-voltage region in the output characteristics (Figure 3c) was attributed to the relatively high contact resistance at the metal/semiconductor interface. Since C_8-BTBT is wide bandgap material and the film has a deep valence band (VB) level (EV = 5.7 eV),[25] a high charge injection barrier can exist at the metal/organic interface due to the energy mismatch between the Fermi level of the Au NP electrodes and the VB of the C_8-BTBT film. In contrast, the drain current in the high-drain-voltage regions shows saturation characteristics, which confirms an ideal MOSFET operation. Figure 3d shows that hysteresis-free transfer characteristics were achieved with a steep increase in drain current in the sub-threshold region. Gate leak current was substantially reduced by complete patterning of the electrode and semiconductor layers (not shown), which allowed an on-off ratio of 10^6. The average μ_{FET} and threshold voltage (V_T) of the fully-printed OTFTs calculated from 20 devices were 7.9 ± 1.1 $cm^2\ V^{-1}\ s^{-1}$ and 1.1 ± 0.4 V, respectively. The variation in these two values may be related to the polycrystalline structure of the C_8-BTBT film and the high contact resistance of the OTFTs as reflected in the nonlinear rise in drain current shown in Figure 3c. For further improvement in performance

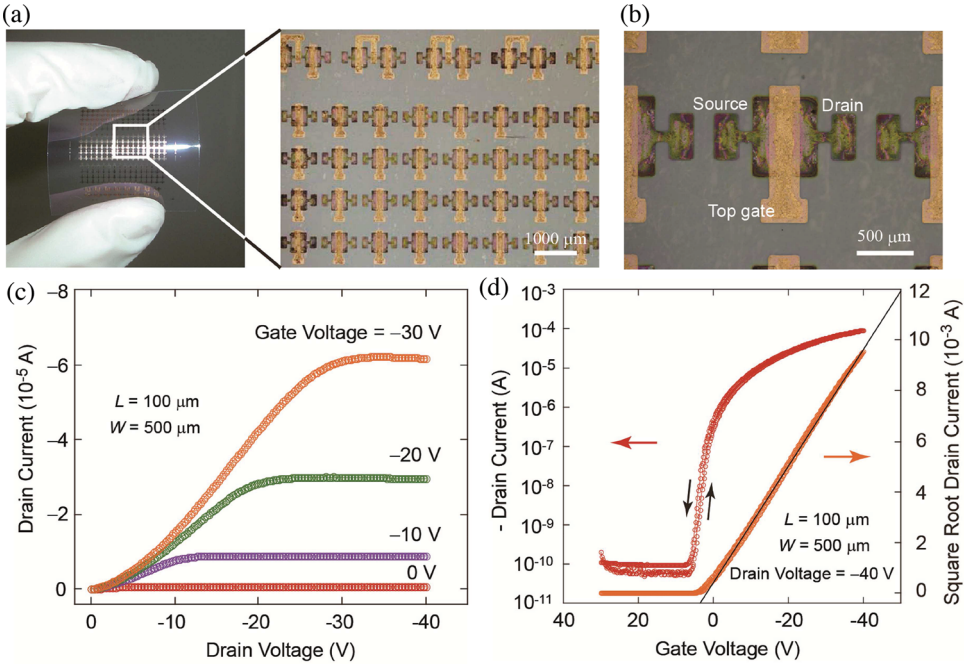

Figure 3. OTFT devices fabricated using the RT printing process on a plastic substrate. a) Flexing the printed OTFT arrays on the plastic substrate (left). Substrate size was 40 × 40 mm^2. An optical microscope image of the OTFT array (right). b) Optical microscope image of the individual device. The electrode and organic semiconductor layers are fully patterned to reduce the off current and cross-talk among the devices. c) Typical output characteristics of the RT printed OTFT. d) Typical transfer characteristics of the OTFT device.

uniformity of the device characteristics, reducing this contact resistance is necessary.

5. Printing of OTFT Arrays on Paper

The proposed fabrication method of organic electronics at RT enables formation of devices on the surfaces of heat-sensitive materials because of the low fabrication temperature. To confirm the superiority of the extremely low-temperature fabrication process, OTFTs were fabricated using paper as the substrate. Paper has been used previously as a substrate for OTFTs using a vacuum evaporation process;[26–28] however, this study produced fully-printed OTFTs on paper. A commercially available photo paper (inkjet printer paper) was selected as the heat-sensitive substrate. This paper degrades at temperatures of approximately 60 °C. Thus, only a RT process could be used to fabricate fully-printed devices on the paper.

First, the logo of our institute was printed on the paper surface using an inkjet printer (**Figure 4**a) to confirm the identity of the substrate as paper. Then the surface was passivated with a parylene layer 3 μm thick, which provided a hydrophobic surface on the paper substrate and reduced surface roughness. Similar procedures used for the plastic substrate also were used to form the devices on the paper. The lines of Au NPs for the source/drain electrodes were patterned by the selective deposition process. Then, an organic semiconductor layer of C_8-BTBT was patterned in the channel region using the combination of screen printing of a guide layer and solution casting of the semiconductor to the defined regions. The polymer gate dielectric layer was formed by spin-coating, followed by drying at RT. Finally, gate lines were drawn by the selective deposition method, and OTFT arrays were successfully formed on the paper substrate. Typical transfer characteristics of the fully-printed OTFTs on paper are shown in Figure 4d. Stable operation of the OTFTs was realized without hysteresis behavior. The average μ_{FET} of the fully-printed OTFTs on the paper was estimated to be 2.5 $cm^2\ V^{-1}\ s^{-1}$.

6. Conclusion

Flexible electronic devices were printed at RT using π-junction Au NP ink as the electrodes, which demonstrated the usefulness of this method as a core technology for flexible printed electronics. The low processing temperature enables use of non-heat-resistive materials as a substrate. The OTFT devices printed at RT had average values for μ_{FET} of 7.9 and 2.5 $cm^2\ V^{-1}\ s^{-1}$ on plastic and paper substrates, respectively, with minimal hysteresis behavior and a V_T near zero. The high μ_{FET} value obtained from the RT-printed OTFTs is comparable to that of IGZO TFTs. In addition, RT printing may be applied to a broader range of thin-film electronic devices, such as light-emitting devices and photovoltaic cells.

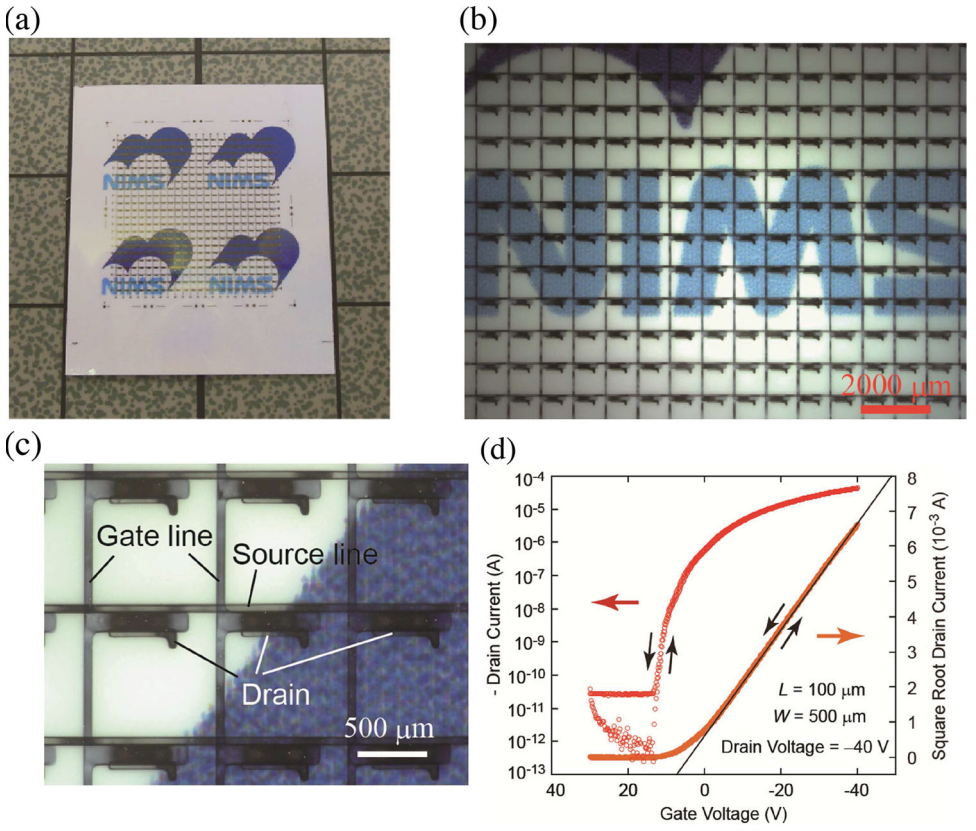

Figure 4. An OTFT active-matrix array assembled on a paper substrate using the RT printing process. a) OTFT array on the paper substrate. The size of the paper was 40 × 50 mm^2. b) Optical microscope image of the OTFT array fabricated using the RT printing technique. c) Enlarged optical micrograph of the RT printed OTFT devices on paper. d) Typical transfer characteristics of the printed OTFTs on paper.

The ability to print plastic electronic devices at RT is expected to promote major advances in electronics production technology, because of several key advantages. Thermal damage is avoided due to the RT process, which allows the use of many flexible substrate types. A flexible substrate is necessary for large-scale roll-to-roll fabrication of devices, thus this RT process provides a method for future printed electronics. Device fabrication based on this simple printing process under ambient conditions is a low-cost and high-throughput process. This advantage can be enhanced by increasing production size and volume. Finally, the methods used to produce the high-performance devices described here can be applied to other practical electronic products. Mass production of devices, such as fully flexible electronic papers or displays, becomes possible because of the flexibility and high mobility of the printed OTFTs. Thus, this RT printing process is a promising method as a core technology for future semiconductor electronics.

7. Experimental Section

Surface Selective Deposition Method: Patterned deposition of Au NP ink was performed using a surface selective deposition method. Surface wettability produced by VUV irradiation was applied to selected regions of the hydrophobic polymer surface using a VUV irradiation system including a VUV excimer lamp (Ushio Inc.) and mask aligner (Figure S1a-b). The wavelength of the light was 172 nm. Selected regions of the polymer surface were exposed to VUV light through a photo mask to render them hydrophilic. Next, the Au nanoparticle ink was applied to the surface with an applicator or a blade coater (Figure S1c). The ink adhered only to the hydrophilic regions to produce patterned Au electrodes (Figure S1d-e). More information can be found in Supplementary Information.

π-Junction Au Nanoparticles: The π-junction Au NP ink is available from Colloidal Ink Co., Ltd. The synthetic procedure for the Au NP ink has been partially reported previously.[18]

Room-Temperature Printing of OTFTs: Fabrication of fully-printed OTFTs was demonstrated on flexible plastic and paper substrates. Polyethylene naphthalate film (Teijin DuPong Film Co. Ltd.) covered with a surface planarizing layer of parylene (3 μm thick) was used as the plastic substrate. For the paper substrate, a parylene layer 3 μm thick was formed on the surface as the passivation layer. The source/drain electrodes of Au NP ink were formed using the surface selective deposition method. Here the source/drain electrode regions were exposed to VUV irradiation (172 nm) through a photo mask for 5 seconds. The VUV irradiation rendered the surface region hydrophilic. Then, Au NP ink was applied to the surface with an applicator to obtain source/drain electrodes on the hydrophilic regions. An organic semiconductor layer was prepared using screen printing and solution casting. A lyophobic layer of Cytop first was formed out of the channel region by screen printing, which then served as the guide for the semiconductor solution. The organic semiconductor solution was prepared by dissolving C_8-BTBT in chlorobenzene at a concentration of 0.5 wt%. The solution was simply drop cast onto the surface, where it crystallized only in the channel regions defined by the Cytop film. This double-layered structure was used for the gate dielectric. The Cytop layer 205 nm thick was formed as the first layer by spin coating to passivate the organic semiconductor/gate dielectric interface and decrease the interfacial trap density. For the upper layer of the gate dielectric, one of two materials, parylene and Fluorosurf, were chosen depending on the situation. A parylene film with a thickness of approximately 300 nm was deposited by chemical vapor deposition using a home-made reactor. Fluorosurf is a fluorinated polymer provided by Fluoro Tech. Co. Ltd., and could be deposited under air without annealing. The material was spin-coated several times to achieve a film thickness of 300 nm. Finally, the top-gate electrode regions were exposed to VUV irradiation through a photo mask to render the surface regions hydrophilic (5 sec for parylene and 60 sec for Fluorosurf), followed by application of Au NP ink using an applicator to obtain the top-gate electrodes. RT printing was used for all of the fabrication processes.

Measurements and Electrical Characterization: Scanning electron microscopic images of the Au NPs were obtained using a S-5200 instrument (Hitachi High Tech.). Film thicknesses were determined using a Surfcorder ET200 instrument (Kosaka Lab.). Electrical characteristics were measured under dark and in a vacuum (10^{-4} Pa) using a B1500A semiconductor device parameter analyzer (Agilent).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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